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09/385,394	08/30/1999	JOHN S. YATES JR.	30585/3	9093

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ELLIS, RICHARD L

ART UNIT	PAPER NUMBER
2183	8

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No. 09/385,394	Applicant(s) Yates Jr. et al.
Examiner Richard Ellis	Group Art Unit 2183

-The MAILING DATE of this communication appears on the cover sheet beneath the correspondence address-

Period for Response

A SHORTENED STATUTORY PERIOD FOR RESPONSE IS SET TO EXPIRE 3 (Three) MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a response be timely filed after SIX (6) Months from the mailing date of this communication.
- If the period for response specified above is less than thirty (30) days, a response within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for response is specified above, such period shall, by default, expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to respond within the set or extended period for response will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).

Status

Responsive to communication(s) filed on November 16, 2000.
 This action is FINAL
 Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under Ex parte Quayle, 1935 C.D. 11; 453 O.G. 213.

Disposition of Claims

Claim(s) 1-95 is/are pending in the application.
 Of the above claim(s) _____ is/are withdrawn from consideration.
 Claim(s) _____ is/are allowed.
 Claim(s) 1-19, 21-34, 37-59, 61-85, and 87-95 is/are rejected.
 Claim(s) 20, 23-26, 60, and 86 is/are objected to.
 Claim(s) _____ are subject to restriction or election requirement.

Application Papers

See the attached Notice of Draftsperson's Patent Drawing Review, PTO-948.
 The proposed drawing correction, filed on _____ is approved disapproved.
 The drawing(s) filed on _____ is/are objected to by the Examiner.
 The specification is objected to by the Examiner.
 The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. § 119(a)-(d)

Acknowledgement is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d).
 All Some* None of the CERTIFIED copies of the priority documents have been received
 received in Application No. (Series Code/Serial Number) _____
 received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

*Certified copies not received: _____

Attachment(s)

Information Disclosure Statement(s), PTO-1449, Paper No(s). 5 and 6 ✓ ✓
 Notice of References Cited, PTO-892 ✓ ✓
 Notice of Draftsperson's Patent drawing Review, PTO-948 ✓

Interview Summary, PTO-413
 Notice of Informal Patent Application, PTO-152
 Other _____

Office Action Summary

1. Claims 1-95 are presented for examination.
2. The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed. The current title is imprecise.
3. Claim 21 is objected to because of the following informalities: The claim terminates with two periods instead of a single period. Appropriate correction is required.
4. The following is a quotation of the appropriate paragraphs of 35 USC § 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless --

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

5. This application currently names joint inventors. In considering patentability of the claims under 35 USC § 103, the Examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR § 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the Examiner to consider the applicability of potential 35 USC § 102(f) or (g) prior art under 35 USC § 103.

6. The following is a quotation of 35 USC § 103 which forms the basis for all obviousness rejections set forth in this Office action:

A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Subject matter developed by another person, which qualifies as prior art only under subsection (f) or (g) of section 102 of this title, shall not preclude patentability under this section where the subject matter and the claimed invention were, at the time the invention was made, owned by the same person or subject to an obligation of assignment to the same person.

7. Claims 1-2 are rejected under 35 USC 102(b) as being clearly anticipated by Richter et al., U.S. Patent 5,481,684.

Richter et al. was cited on applicants information disclosure statement, paper number 6, filed November 16, 2000.

Richter et al. taught (e.g. see figs. 1-5) the invention as claimed (as per claim 1), including a data processing ("DP") system comprising:

- A) a computer (fig. 5), comprising: a processor pipeline (62, 66, 48) designed to alternately execute instructions coded for first and second different computer architectures or coded to implement first and second different processing conventions (col. 1 line 61 to col. 2 line 12);
- B) a memory for storing instructions for execution by the processor pipeline (col. 2 lines 5-6), the memory being divided into pages for management by a virtual memory

manager (col. 6 lines 50-53), a single address space of the memory having first and second pages (inherent from the definition of a paged virtual memory);

- C) a memory unit designed to fetch instructions from the memory (fig. 5, 62) for execution by the pipeline, and to fetch stored indicator elements associated with respective memory pages of the single address space from which the instruction are to be fetched (col. 2 lines 1-6), each indicator element designed to store an indication of which of two different computer architectures and/or execution conventions under which instruction data of the associated page are to be executed by the processor pipeline (fig. 4, col. 8 line 61 to col. 9 line 9);
- D) the memory unit and/or processor pipeline further designed to recognize an execution flow from the first page, whose associated indicator element indicates the first architecture or execution convention, to the second page, whose associated indicator element indicates the first architecture or execution convention, and in response to the recognizing, to adapt a processing mode of the processor pipeline (or) a storage content of the memory to effect execution of instructions in the architecture and/or under the convention indicated by the indicator element corresponding to the instruction's page (col. 8 line 61 to col. 9 line 57).

8. As to claim 2, Richter et al. taught that the two architectures are two instruction set architectures (col. 1 lines 61-67); and

wherein the adapting step included controlling instruction execution hardware of the computer to interpret the instruction according to the two instruction set architectures according to the indicator elements (col. 9 lines 2-57).

9. As to claims 4-18, 21-28, 30-33, 37-59, 61-75, 77-78, and 94, they do not teach or define above the invention claimed in claims 1-2 and are therefore rejected under Richter et al. for the same reasons set fourth in the rejection of claims 1-2, supra.

10. As to claim 8, Richter et al. taught that the entries were entries in a TLB (fig. 3, 33, col. 10 lines 50-67).

11. As to claim 9, Richter et al. taught presence of an instruction cache (col. 29, "icbi").

Due to the definition of an instruction cache, it would be inherent that it would have held regions of program code in storage lines.

12. As to claim 17, Richter et al. taught that one of the regions stored an off-the-shelf operating system binary coded in an instruction set non-native to the computer, the non-native instruction set providing access to a reduced subset of the resources of the computer (col. 9 lines 42-57).
13. As to claim 21, Richter et al. taught that the instruction data coded for execution by a first of the two instruction set architectures observes a data storage convention associated with the first architecture, and instruction data coded for execution by a second of the two instruction set architectures observes a second, different, data storage convention associated with the second architecture, a single indicator element indicating both the instruction set architecture and the data storage convention (col. 9 lines 18-26), and recognizing when program execution transfers from a region using the first instruction set architecture to a region using the second instruction set architecture, and in response to the recognition, adjusting the data storage content of the computer from the first storage convention to the second (col. 9 lines 22-26).
14. As to claims 24-27, Richter et al. taught altering a bit representation of a datum from a first representation in the first convention to a second representation in the second convention, the alteration of representation being chosen to preserve the meaning of the datum across the change in execution convention (col. 9 lines 17-26).
15. As to claim 94, Richter et al. taught executing a set of computer object code twice, without modification of the data values making up the code, while providing two different outcomes from execution of that code due to the execution occurring within one of two different instruction set architectures (col. 13 line 48 to col. 14 line 5).
16. Claims 3, 19, 29, 76, 79-85, 87-93 and 95 are rejected under 35 USC § 103 as being unpatentable over Richter et al., as applied to claims 1-2, 4-18, 21-28, 30-33, 37-59, 61-75, 77-78, and 94, supra.
17. Richter et al. did not specifically teach that the system transformed a calling convention

of a first architecture into a calling convention of a second architecture. However, Richter et al. did teach the necessity of transforming aspects specific to one architecture into the appropriate aspect specific to the other architecture, due to the need to maintain compatibility between the two architectures (col. 9 lines 17-26). As calling conventions, and specifically, register based vs. stack based calling conventions, are notoriously well known in the prior art, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to have implemented calling convention transformation within Richter et al.'s system because doing so would be required in order to produce a processor that is properly capable of performing as Richter et al. desired, e.g., with one architecture calling routines coded in the other architecture (col. 9 lines 27-57).

18. Claims 20, 34-36, 60, 86 are objected to as being dependent upon a rejected base claim, but would render the base claim allowable if bodily incorporated into the base claim such that the new base claim included all of the original limitations of the base claim, any intervening claims, and the objected claim.
19. The prior art made of record and not relied upon is considered pertinent to Applicant's disclosure.
20. A shortened statutory period for response to this action is set to expire 3 (three) months and 0 (zero) days from the mail date of this letter. Failure to respond within the period for response will result in **ABANDONMENT** of the application (see 35 USC 133, MPEP 710.02, 710.02(b)).
21. Any inquiry concerning this communication or earlier communications from the Examiner should be directed to Richard Ellis whose telephone number is (703) 305-9690. The Examiner can normally be reached on Monday through Thursday from 7am to 5pm.

If attempts to reach the Examiner by telephone are unsuccessful, the Examiner's supervisor, Eddie Chan, can be reached on (703) 305-9712. The fax phone numbers for this Group are: After-final: (703) 746-7238; Official: (703) 746-7239; Non-Official/Draft: (703) 746-7240.

Any inquiry of a general nature or relating to the status of this application should be directed to the Group receptionist whose telephone number is (703) 305-3900.

Richard Ellis
February 13, 2002



Richard Ellis
Primary Examiner
Art Unit 2183